Curriculum Vitae

1) Name : **DR. PARESH JAYCHAND SHAH**
2) Designation : Professor
3) Date of Birth : 11/08/1967
4) Resi. Address : Jay, Plot No.23, Gat No.28, Near Hanuman Mandir, Muktai Nagar Colony, JALGAON – 425 001 (M.S.)
5) E-mail ID : pjshahj@yahoo.com
6) Telephone No. : 098900 94045, 0257-2254250 (R)
7) Sex : Male
8) Nationality : Indian
9) Qualifications :-

Sr. No.	Educational Qualifications	Name of Institute	Name of University/Board	Passing Year	Class Obtained
	Ph. D.	SGSITS, Indore	RGPV, Bhopal	22/11/2014	Awarded
1	M. E. (Power Electronics)	SGSITS, Indore	DAVV, Indore	May 1997	First Class with Distinction
2	B.E. (Ind. Electronics)	SSGMCE, Shegaon	Amravati Univ.	May 1989	First Class
3	H.S.C	Municipal High., Malkapur	Nagpur Board	May 1985	Second Class
4	S.S.C.	LBC Vidyalay, Malkapur	Nagpur Board	May 1983	First Class
5	D.B.M.	NMIM, Jalgaon	Pune	Aug. 1992	First Class
6	M.M.S.	NMIM, Jalgaon	N.M.U.	Sep. 1993	First Class
7	A.D.C.S.S.A.A.	Govt. Poly., Jalgaon	D.T.E.,Mumbai	Aug. 1999	First Class

10) **Ph.D. Thesis :-**

A) Supervised By :- Prof. Rakesh Saxena, S.G.S.I.T.S.,Indore

B) Topic :- Power Quality Improvement & Filtering Techniques in Power Supplies.

11) **M.E. Dissertation :-**

A) Supervised By :- Dr. C.V. Abrol & Prof. M.P.S.Chawla, S.G.S.I.T.S.,Indore

B) Topic :- Software Based Speed Control of Non-Linear DC drive with continuous control & Variable Structure Control

12) **Experience:- 27 Years and 6 months on 31/03/2017.**

A) In Chronological order starting from the present Job.

Designation	**Employer**	**Duration**	**Exp. in Yrs. m**	**Scale**	**Basic**
Professor	SSBT's COET, Jalgaon	Since 01/01/2015	2.3	37000-0-67000 (AGP 10,000)	63,573/-
Head of Department	Electrical Engg. Deptt., SSBT's COET, Jalgaon	Since 19/01/2015	2.3	-	-
Associate Professor	SSBT's COET, Jalgaon	01/03/10 to 31/12/15	4.10	37000-0-67000 (AGP 9,000)	57,838/-
Assistant Professor	SSBT's COET, Jalgaon	01/12/02 to 28/02/10	7.3	12000-420-18300	17,040/-
Lecturer	SSBT's COET, Jalgaon	17/07/90 to 30/11/02	12.5	8000-275-13500	9,100/-
Trainee Engineer	Asapura Television, Jalgaon	01/01/90 to 30/06/90	0.6	2000	-
Trainee Engineer	M/S Chowgule Engineers & Machines Ltd. Thane.	21/08/89 to 31/10/89	0.3	1200	-

B) As a Lecturer or equivalent (in years and months):- 12 Years, 05 Months

C) Experience as 'Assistant Professor' (in years and months):-07 Years,03 Months

D) Experience as 'Associate Professor' (in years and months):-04 Years,10 Months

E) Experience as 'Professor' (in years and months):- 02 Year,03 Months

F) **BOS Chairman of Electrical Engineering** and Instrumentation Engineering at NMU, Jalgaon

G) Details of approval / University reference :

i) Approved **Assistant Professor** (Lecturer in old scale) from **09/02/2004** with **Ref. no**.NMU/18/J-4/644/2006 date:20/03/2006.

ii) Approved **Associate Professor** (Assistant Professor in old scale) from **22/06/2009** with **Ref. no**.NMU/18/1074/2009 date:10/09/2009.

iii) Approved **PGTeacher** from **08/11/2013** with **Ref. no.** NMU/11/PGR/Elect. Engg./2410/2013 dated:18/11/2013.

13) Job responsibility :- Head of Department, Teaching honestly, UG & PG Teacher, UG & PG guide, NBA work, NAAC work, Publishied/present research papers in Journals and conferences, Attended conference/workshops/seminars, Admission committee member, Organized workshop, University/inter university work like: chairman of flying squad, LIC committee member, senior supervisor, paper setting, paper assessment, prepared curriculums, practical exams etc, Chairmen of sports committee, ARC incharge, Lab developments, Lab in charge, Time Table coordinator, Conducting students association activities as a faculty advisor like: Blood donation camp, Expert lectures, Conducted Paper Presentation, Conducted Alumni meet etc.

14) **Membership of Professional bodies. : -**

1) Life Membership of **ISTE.** (LM 24804)
2) Life Membership of **IE (I)** (M 123291/0)
3) Membership of **ISLE** (S 0511)

15) Language known: English, Hindi, Marathi, Kutchhi, Gujrati

16) **List of Research work & publications**: 45+ Research papers published in International/ national Journals and conferences.

A) List of foremost publications from 2009 to 2016:

1. **P. J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Digital control technologies for improving the power quality of power supplies," Neural computing and applications, **Springer International Journal**, vol.22, no. 1, pp. 235-248, May 2013.
   [Science Citation Index Expanded (SciSearch), Journal Citation Reports/Science Edition, SCOPUS, INSPEC, Zentralblatt Math, Google Scholar, EBSCO, CSA, Academic OneFile, Academic Search, ACM Digital Library, Computer Science Index, CSA Environmental Sciences, Current Contents/Engineering, Computing and Technology, DBLP, EI-Compendex, Gale, io-port.net, OCLC, PASCAL, Referativnyi Zhurnal (VINITI), SCImago, STMA-Z, Summon by ProQuest**]**
2. **P. J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Digital filter design with harmonics estimation for power supplies," **Springer-Journal of the Institution of Engineers (India): series B**, vol.93, no.2, pp. 73-79, *July 2012*.(ISSN: 2250-2160, DOI: 10.1007/s40031-012-0014-z) **[**Google Scholar, EBSCO, OCLC, Summon by ProQuest]
3. **Paresh J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Artificial intelligence approaches to advance signal processing and simulation methods for efficient power supplies," International journal of electrical and electronic engineering - **Scientific And Academic Publishing** (SAP), vol.2, no.4, pp. 217-225, August 2012.(DOI: 10.5923/j.eee.20120204.07) **[**Zentralblatt Math, Google Scholar, EBSCO, CASSI]
4. **Paresh J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Design and modeling of a digital controller for SMPS," International journal for power electronics and energy – **Consortium of Advanced Science and Engineering** (IJPEE - CASER), vol. 1, no. 1, pp. 10-18, July 2012.(ISSN: ABCD-WXYZ) **[**Zentralblatt Math, Google Scholar, EBSCO]
5. **Paresh J. Shah**, Rakesh Saxena, M. P. S. Chawla, "FPGA based digitalized power supplies," IEEE fifth India international conference on power electronics (IICPE 2012), Delhi technological university, Delhi, India, pp. 78, Dec. 6-8, 2012 (**Available on IEEE Explorer**).

6. **Paresh J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Power Quality Improvement in Switch Mode Power Supply using FPGA based Digital Control Approaches," **Elsevier & ACEEE** Fourth International joint conference on advances in engineering and technology, NCR, India, pp. 645-652, Dec. 13-14, 2013 (Published in Elsevier proceedings).
7. **P. J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Power quality requirement for uninterruptible power supplies," IEEE international conference on computational intelligence, communication systems and networks (CICSyN 2009), Indore, Madhya Pradesh, pp. 53, 23-25 July 2009.
8. **P. J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Various techniques for improving the power quality in power supplies," IEEE international conference on computational intelligence, communication systems and networks (CICSyN 2009), Indore, Madhya Pradesh, pp. 58, 23-25 July 2009.
9. **P. J. Shah**, Rakesh Saxena, M. P. S. Chawla, "Review of signal processing methods for power quality improvement," International conference on electrical power and energy systems (ICEPES – 2010), MANIT, Bhopal, Madhya Pradesh, pp. 129-134, 26-28 August 2010.
10. Dinesh Ahirrao, Praful Pachpande, **Paresh Shah**, "Counter Based DPWM Single Phase Inverter using FPGA", International conference, Icost 2011, SSVPS, Dhule, pp. 7.12.1 - 712.6, Jan 13- 15, 2011.
11. **P. J. Shah**, Gunjal Oza, Digitally controlled power electronics converters, National conference on emerging technology in engineering and management, NATCOC-2011, Godawari Engg. College, Jalgaon, pp. 2, 20 Feb 2011.
12. Gunjal Oza, Dhanshri Patil, **P. J. Shah**, "Digital filter design with harmonics estimation analysis for power electronics converters", National conference, Milstone2k11, SSBT's COET, Jalgaon, 29 March, 2011.
13. Shubhangi Patil, Tejashri Shikla, **Paresh J. Shah**, "Modeling of PID controller based SMPS using FPGA", International Journal of Innovative Research in Science, Engineering and Technology, Vol. 1, Issue 2, pp 159-168, December 2012.
14. Shubhangi Patil, **Paresh J. Shah**, "PID Controller based model for DC-DC Buck Converter, National conference", IEEE national conference on technological research in electrical and electronics engineering, TRIEECON-2012, Shri Aurobindo Institute of Technology, Indore, pp. 2, Oct. 9-10, 2012.(ISSN: 2319-8753)
15. Tejashri Shikla, **Paresh J. Shah**, "FPGA Based Space vector PWM - Multilevel Inverter" IEEE national conference on technological research in electrical and electronics engineering,

TRIEECON-2012, Shri Aurobindo Institute of Technology, Indore, pp. 4, Oct. 9-10, 2012.

16. Tejashri R. Shukla, **Paresh J. Shah**, "Simulation of single phase digital PWM inverter with boost PFC techniques," International journal of engineering science, TI journal, vol. 4, no. 3, pp. 45-50, March 2015.(ISSN: 2306-6474)
17. Priyanka Mahajan, **Dr. P. J. Shah**, "Designing and analysis of power system with SFCL module" 2nd International conference of advances in engineering & technology, Nagpur, vol. 2, pp. 152-156, Feb 25-26, 2015.
18. Priyanka Mahajan, **Dr. P. J. Shah**, "Designing and analysis of power system with SFCL module" International Journal on Recent and Innovation Trends in Computing and Communication, vol.3, issue 2, pp. 78-82, March 2015.(ISSN: 2321-8169, Impact factor 5.098)
19. Gauri S. Sarode, **Dr. Paresh J. Shah**, Dr. Rakesh Saxena, "Overview of interline dynamic voltage restorer for power quality improvement", Australian Journal of Information Technology and Communication, Volume 2, Issue 1, pp. 16-20, April 10, 2015.(ISSN: 2203-2843) Impact Factor 0.78.
20. Gauri S. Sarode, **Dr. Paresh J. Shah**, Dr. Rakesh Saxena, "Modeling and Evaluation of Interline Dynamic Voltage Restorer for Distribution System", Pratibha: International Journal of Science Spirituality business and technology, vol. 3, no. 2, pp. 61-65, June 2015.
21. Priyanka Mahajan, **Dr. Paresh J. Shah**, Dr. Rakesh Saxena, "Analysis of smart grid with superconducting fault current limiters", Pratibha: International Journal of Science Spirituality business and technology, vol. 3, no. 2, pp. 87-92, June 2015.
22. Sagar Joshi, **Dr. Paresh J. Shah,** "An Overview of Voltage Stability of DFIG wind generation system during Faults by DVR", Pratibha: International Journal of Science Spirituality business and technology, vol. 3, no. 2, pp. 10-15, June 2015.
23. Priyanka Mahajan, **Dr. Paresh J. Shah**, Dr. Rakesh Saxena, "Analysis the response of single and multiple superconducting fault current limiters in smart grid for symmetrical fault ", International Journal of Engineering and technology, vol. 5, no. 7, pp. 417-425, July 2015 (ISSN: 2049-3444) [IET., google, Engg & technology, Doaj, CAS etc].
24. Gauri S. Sarode, **Dr. Paresh J. Shah**, "Voltage Sag Compensation Capacity of IDVR", European Journal of Advance in Engineering and Technology, vol. 2, no. 7, pp. 48-55, August 2015 (ISSN: 2394-658X). [Cross ref, IJEAT etc.]
25. Sagar P. Joshi. **Paresh J. Shah**, "Topology for voltage sag and swell compensation by dynamic voltage restorer", International Journal of Innovation Research in Electrical,

Electronics, Instrumentation and Control Engineering, vol. 3, issue 11, pp. 50-53, November 2015. (Impact factor 3.885) [get cited, index Copernicus, world cat, google scholar]

26. Sagar P. Joshi. **Dr. Paresh J. Shah**, "Voltage Sag Compensation by DVR for DIFG wind turbine system", International Journal of Recent and Innovation trends in computing and communication, vol. 3, issue 12, December 2015. (Impact factor 5.837)
27. Rohit Firke, **Dr. Paresh J. Shah**, " Compensation of reactive power and harmonics by using DSTATCOM", International Conference on Global Trends in Engineering, Technology and Management 2016, Jalgaon, pp. 437-440, Jan. 2016.
28. Gaurav B. Patil, **Paresh Shah**, "Comprehensive Study of Forward and Fly Back Converter for Improvement in Performance" International Journal of Science and Research (IJSR), Volume 5, Issue 3, pp. 1644-1648, March 2016 (ISSN: 2319-7064, Index Copernicus Value (2013): 6.14, Impact Factor (2014): 5.611).
29. Madhuri N. Kshirsagar, **Dr. P. J. Shah**, "A Review of the single Phase Transformer Less Full Bridge PV Grid Inverters" IJSRD - International Journal for Scientific Research & Development| Vol. 4, Issue 02, pp. 1860-1864. April 2016 (ISSN (online): 2321-0613, Impact factor 2.39, indexing- Scribd, google scholar, academia.edu, issuu, research bible)
30. Madhuri N. Kshirsagar, **Dr. P. J. Shah**, "Evaluation of Transformerless Inverters for Single Phase Photovoltaic Systems" IJIREEICE International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering Vol. 4, Issue 6, pp. 139-145, June 2016 (ISSN-Online 2321–2004, ISSN-Print 2321–5526, Impact factor 5.621, indexing- science central.com, scirate.com, Scribd, google scholar, scientific commons, J-gate, research bible etc.)
31. Gaurav B. Patil, **Dr. Paresh Shah**, "Single Stage Forward-Flyback Converter for Improvement in Performance" International Journal of Engineering Science and Computing (IJESC), Volume 6, Issue 7, pp. 1587-1592, July 2016 (ISSN: 2321-3361, Peer Reviewed, Impact Factor: 5.611, indexing- academia.edu, cite factor, index copernicus international, paperity, science central.com, sciseek, science directory, google scholar, scientific commons etc.)
32. Madhuri Kshirsagar, Dr. P. J. Shah "High Efficiency H6 Transformerless topology based Single Phase Full Bridge PV Grid tied Inverters" Asian Journal of Science and Technology, Vol.7 issue 11, pp.3837- 3841, Nov. 2016.

B) Resarch Proposals

1. Proposal for research project "Detection and analysis of the power quality problems of different systems and improvements" under the scheme "UGC – FRPS Start-Up Grant Project" is submitted to UGC.

2. Proposal for research project "High Voltage Direct Current (HVDC) Transmission Model" submitted to VCRMS on 19th January 2017.
3. Proposal for research project "Boost Rectifier with Power Factor Correction (PFC)" submitted to VCRMS on 19th January 2017.

C) Reviewer of International / National Journal/conferences: 7

1. SAP International Journal of Microelectronics and Solid State Electronics
2. SAP International Journal of Electrical and Electronic Engineering
3. SAP International Journal of Energy and Power
4. IEEE conference WICT 2011
5. IEEE conference IICPE 2012
6. IEEE conference CICN 2012
7. IEEE conference ICSPICC 2016
8. Pratibha International Journal
9. IEEE conference ICSPICC-2016

D) Books written:

1. Power Electronics
2. VLSI Design

17) List of a) conference/seminars b) workshop/Symposium c) winter school/summer school attended :- **(**Total 21 Weeks & 23 Days= 25 Weeks**)**

Sr. No.	Workshop/ Seminars.	Duration	Weeks	Subject	Place
1	Winter school S.T.T.P	Nov 4-15, 1997	2	Advances Power Electronics	V.R.C.E., Nagpur
2	Summer school S.T.T.P	May 11-30, 1998	3	Induction Training Programme	A.M.U., Aligarh
3	Seminar	Aug 11- 17,1998	1	Topic Related to Engineering Education	SSBT's COET, Jalgaon
4	Seminar	Dec 26, 1998	1 Day	Quality Engineering Education	SSBT's COET, Jalgaon
5	Summer school S.T.T.P	June 12-24, 2000	2	Recent Advances in Power Electronics & its Application	M.R.E.C., Jaipur
6	Winter school S.T.T.P	Dec 26,2000 –Jan 4, 2001	2	Induction Training for Technical Teachers	J.T.M.C.O.E., Faizpur
7	Workshop	Jan 25, 2003	1 Day	Syllabus Revision	S.S.V.P.S.C.O.E., Dhule
8	Workshop	July 10 –13, 2003	1	Orientation Program for Engineering College Teachers	SSBT's COET, Jalgaon
9	Workshop	July 22 –23, 2003	2 Days	MATLAB & Simulink	SSBT's COET, Jalgaon
10	Winter school S.T.T.P	Nov 17-29, 2003	2	VLSI Circuit Design using HDL	Priyadarshini C.E., Nagpur
11	Certificate Course	July 5-11, 2004	1	VLSI Design	Bit Mapper, Pune
12	Workshop	July 31, 2006	1 Day	Syllabus Framing of Engg. Faculty	SSBT's COET, Bambhori, Jalgaon
13	National Seminar	April 21, 2007	1 Day	Low Cost Automation	SSBT's COET, Jalgaon
14	Workshop	July 26-28, 2007	3 Days	Adv. Commu.Embedded System, Image Processing, VLSI	S.S.V.P.S.C.O.E., Dhule
15	STTP	July 7-11, 2008	1	Recent Trends in Power Electronics	S.V.N.I.T., Surat

16	Work shop	July 22-23, 2008	2 Days	VLSI Design	SSBT's COET, Jalgaon
17	STTP	March 30 - April 3, 2009	1	Emerging Trends in DSP & Communication	SSBT's COET, Jalgaon
18	Workshop	July 9-11, 2009	3 Days	Teachers training workshop	SSBT's COET, Jalgaon
19	Workshop	July 17, 2009	1 Day	ME E & TC (Digital Electronics) Syllabus Framing of Engg. Faculty	SSBT's COET, Jalgaon
20	Training Programme	Jan 23, 2010	1 Day	Disaster Management	SSBT's COET, Jalgaon
21	Workshop	April 23, 2010	1 Day	Lightning trends & technologies vision 2020	ISLE, Hotel Fortune Landmark, Indore
22	Workshop	July, 24, 2010	1 Day	Syllabus Framing for post graduate in Electronics & Tele. Engg.	SSGB's COE, Bhusawal
23	STTP	June, 4-8, 2012	1	Advanced Power Electronics & real time digital controller	MANIT, Bhopal
24	Workshop	Oct.20, 2012	1 Day	Syllabus framing of SE E&TC for NMU, Jalgaon.	SSBT's COET, Jalgaon
25	STTP	June, 24-28, 2013	1	Real time implementation of Power Electronics technologies	MNIT, Jaipur
26	STTP	Dec 29, 2014 - Jan 2, 2015	1	Implementation of Power Electronics system	S.V.N.I.T., Surat
27	STTP	Dec 7, 2015 – Dec 11, 2015	1	Implementation of Power Electronics Systems	S.V.N.I.T., Surat
28	Workshop	Oct.8, 2015	1 Day	On Sreen Evaluation	SSBT's COET, Jalgaon
29	Workshop	Feb. 5, 2016	1 Day	Solar Activities	kWatt solutions Pvt. Ltd., IIT, Bombay
30	Workshop	March 12, 2016	1 Day	Industrial Automation	SSBT's COET, Jalgaon
31	STTP	Dec 26- 30, 2016	1	Power Conditioning and Distributed Power Generation	S.V.N.I.T., Surat

Any other:

i Received **"Shikshs Ratan Puraskar"** on 08/09/10 at New Delhi.

ii **Google Scholar** citation is 37, and h index is 4.

iii Biography is selected for **"Who's Who in the World 2015".**

iv Received **super genies award at Mumbai**.

v Received the **letter of recognition for 100% results**

vi Institute has secured **top 10 positions in university sports** amongst 250 colleges & **first position amongst all engineering colleges** in 2011-12 under my Chairmanship of sports committee.

vii My project groups' students have received **first prizes in various competitions**.

Result of the subject taught:

1) VLSI Design - B.E. (E&TC): Average Result**: 95.43 %**

Year	Result	
	A Section	**B Section**
2009-10	**100 %**	**100 %**
2010 - 11	**97.01 %**	**93.33 %**
2011-12	**89.04 %**	**98.38 %**
2012 - 13	**89.04 %**	**96.70 %**

2) Power Electronics - T.E. (E&TC): Average Result: **77.65 %**

Year	Result	
	A Section	B Section
2009 - 10	80.82 %	-
2010 - 11	70.10 %	-
2011 - 12	-	88.40 %
2012 - 13	67.40 %	77.02%
2016 - 17	82.14 %	

3) Analog & Digital Electronics (Current year) S.E. (Electrical Engineering) sem-II (2015-16): **96.00 %**

I solemnly declare that the information given above is true to the best my knowledge.

Yours truly

Place :- Jalgaon

Dr. Paresh J. Shah